wherein said switching circuit is electronically switchable to aggregate said photodetector signals according to at least two different selectable pixellization schemes with differing resolutions, such that said switching circuit combines photodetector signals according to at least two different, electronically selectable configurations: a first configuration in which each pixel output is a sum of the outputs of two neighboring photodiodes from within a single pixel; and a second configuration in which each pixel output is a sum of at least three photodiodes; and

a plurality of addressable interface circuits, each of which enables the aggregated pixel output stored on a respective one of said pixel's to be read out in response to an address input.

15. (thrice amended) A photodetector array, comprising a plurality of active pixels, said array of pixels comprising a plurality of pixels arranged into at least three horizontal rows and vertical columns,

wherein each pixel comprises an association of at least two subpixels arranged such that their outputs may be switchably connected to a common pixel node;

and wherein the outputs of said subpixels are switchably combined into at least two different grouping arrangements, to give at least two different selectable pixel resolutions, wherein said at least two different grouping arrangements comprises two different grouping arrangements, one of which combines the outputs of two adjacent subpixels in a given vertical column, and the other of which combines the outputs of three adjacent subpixels in said given vertical column,

each of said pixels having an intrinsic capacitance which stores said combined subpixel outputs prior to their being read out, and